REMARKS

The October 11, 2005 Office Action was base on pending Claims 1-11 and 13-21. This amendment amends Claims 1, 5, and 11. Thus, after entry of the Amendment, Claims 1-11, and 13-21 are pending and presented for further consideration.

In the October 11, 2005 Office Action, the Examiner rejected Claims 1, 3-5, 7, 8, 10, 11, and 13-21 under 35 U.S.C. § 102(b/e) as being anticipated by U.S. Patent No. 5,303,192 ("the Baba patent") or U.S. Patent No. 6,011,710 ("the Wiggers patent"). The Examiner further rejected Claims 2, 6, and 9 under 35 U.S.C. § 103(a) as being unpatentable over the Baba patent or the Wiggers patent.

REJECTION OF CLAIMS 1, 3-5, 7, 8, 10, 11 AND 13-21 UNDER 35 U.S.C. § 102(b)

The Examiner rejected Claims 1, 3-5, 7, 8, 10, 11, and 13-21 under 35 U.S.C. § 102(b) as being anticipated by the Baba patent. In view of the following discussion, Applicant respectfully traverses this rejection.

Claims 1, 5, 11

Baba does not teach decoupling the data bus from the memory integrated circuit to reduce data bus capacitance when the memory integrated circuit is not being accessed. Indeed, Baba teaches decoupling the data bus from a defective memory cell when the memory chip is being accessed.

In contrast, in an embodiment of the invention, a method of making a memory module comprises interfacing a state decoder with a host system comprising a memory controller. The memory controller produces control signals, where the control signals comprise at least one of a row address strobe (RAS), a column address strobe (CAS), and a write enable (WE). The state decoder decodes the control signals to determine whether the memory integrated circuit is being accessed and produces a gate control signal to selectively control the bus switch. In response to the gate control signal, the bus switch decouples the data bus from the memory integrated circuit when the memory integrated circuit is not being accessed to reduce data bus capacitance.

The reference cited by the Examiner does not disclose, teach, or suggest the use of interfacing a state decoder with a host system comprising a memory controller,

the memory controller producing control signals, where the control signals comprise at least one of a row address strobe (RAS), a column address strobe (CAS), and a write enable (WE), where the state decoder decodes the control signals to determine whether the memory integrated circuit is being accessed and produces a gate control signal to selectively control the bus switch, where, in response to the gate control signal, the bus switch decouples the data bus from the memory integrated circuit when the memory integrated circuit is not being accessed to reduce data bus capacitance, and where the interfacing does not provide the gate control signal to the bus switch. Applicant asserts that Claim 1 is not anticipated by the Baba patent. Applicant therefore respectfully submits that Claim 1 is patentably distinguished over the cited reference and Applicant respectfully requests allowance of Claim 1.

Claim 5

Although Claim 5 has different language than Claim 1, Claim 5 is believed to be patentable for similar reasons (where applicable), and because of the different features recited therein.

Claim 11

Although Claim 11 has different language than Claim 1, Claim 11 is believed to be patentable for similar reasons (where applicable), and because of the different features recited therein.

Claims 3, 4, 7, 8, 10, and 13-21

Claims 3, 4, and 13-16, which depend from Claim 1, and Claims 7, 8, 10, and 17, which depend from Claim 5, and Claims 18-21, which depend from Claim 11, are believed to be patentable for the same reasons articulated above with respect to Claims 1, 5 and 11, respectively, and because of the additional features recited therein.

REJECTION OF CLAIMS 1, 3-5, 7, 8, 10, 11, and 13-21 UNDER 35 U.S.C. § 102(e)

The Examiner rejected Claims 1, 3-5, 7, 8, 10, 11, and 13-21 under 35 U.S.C. § 102(e) as being anticipated by the Wiggers patent. In view of the following discussion, Applicant respectfully traverses this rejection.

Claim 1

The memory controller in Wiggers has the disadvantage that an unconventional signal line for gate control needs to be created and routed to the memory module. In contrast, in an embodiment of the invention, the memory module can be placed in an existing convention memory application without any modification of the memory module to memory controller interface, as the state decoder produces the gate control signal. See page 8 lines 24-31 of the specification.

Further, in contrast, in an embodiment of the invention, a method of making a memory module comprises interfacing a state decoder with a host system comprising a memory controller. The memory controller produces control signals, where the control signals comprise at least one of a row address strobe (RAS), a column address strobe (CAS), and a write enable (WE). The state decoder decodes the control signals to determine whether the memory integrated circuit is being accessed and produces a gate control signal to selectively controls the bus switch. In response to the gate control signal, the bus switch decouples the data bus from the memory integrated circuit when the memory integrated circuit is not being accessed to reduce data bus capacitance, and where the interfacing does not provide the gate control signal to the bus switch.

The reference cited by the Examiner does not disclose, teach, or suggest the use of interfacing a state decoder with a host system comprising a memory controller, the memory controller producing control signals, where the control signals comprise at least one of a row address strobe (RAS), a column address strobe (CAS), and a write enable (WE), where the state decoder decodes the control signals to determine whether the memory integrated circuit is being accessed and produces a gate control signal to selectively control the bus switch, where, in response to the gate control signal, the bus switch decouples the data bus from the memory integrated circuit when the memory integrated circuit is not being accessed to reduce data bus capacitance, and where the interfacing does not provide the gate control signal to the bus switch.

Applicant asserts that Claim 1 is not anticipated by the Wiggers patent. Applicant therefore respectfully submits that Claim 1 is patentably distinguished over the cited reference and Applicant respectfully requests allowance of Claim 1.

Claim 5

Although Claim 5 has different language than Claim 1, Claim 5 is believed to be patentable for similar reasons (where applicable), and because of the different features recited therein.

Claim 11

Although Claim 11 has different language than Claim 1, Claim 11 is believed to be patentable for similar reasons (where applicable), and because of the different features recited therein.

Claims 3, 4, 7, 8, 10, and 13-21

Claims 3, 4, and 13-16, which depend from Claim 1, and Claims 7, 8, 10, and 17, which depend from Claim 5, and Claims 18-21, which depend from Claim 11, are believed to be patentable for the same reasons articulated above with respect to Claims 1, 5 and 11, respectively, and because of the additional features recited therein.

REJECTION OF CLAIMS 2, 6, AND 9 UNDER 35 U.S.C. § 103(a)

The Examiner rejected Claims 2, 6, and 9 under 35 U.S.C. § 103(a) as being unpatentable over the Baba patent or the Wiggers patent.

Claim 2, which depends from Claim 1, and Claims 6 and 9, which depend from Claim 5, are believed to be patentable for the same reasons articulated above with respect to Claims 1 and 5, respectively, and because of the additional features recited therein.

REQUEST FOR TELEPHONE INTERVIEW

Pursuant to M.P.E.P. § 713.01, in order to expedite prosecution of this application, Applicant's undersigned attorney of record hereby formally requests a

telephone interview with the Examiner as soon as the Examiner has considered the effect of the arguments presented above. Applicant's attorney can be reached at (949) 721-2998 or at the number listed below.

CONCLUSION

Although amendments and cancellations have been made, no acquiescence or estoppel is or should be implied thereby. Rather, the amendments and cancellations are made only to expedite prosecution of the present application, and without prejudice to presentation or assertion, in the future, of claims on the subject matter affected thereby. Furthermore, any arguments in support of patentability and based on a portion of a claim should not be taken as founding patentability solely on the portion in question; rather, it is the combination of features or acts recited in a claim which distinguishes it over the prior art.

Applicant has endeavored to address all of the Examiner's concerns as expressed in the outstanding Office Action. In light of the above remarks, reconsideration and withdrawal of the outstanding rejections is specifically requested.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

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Dated: Jan 10, 2006

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